ABSTRACT

A semiconductor integrated circuit device including a dynamic random access memory (DRAM) unit having improved signal-to-noise ratio, reduced bit line capacitance, and reduced area is provided. The DRAM unit includes a plurality of bit line pairs, each bit line pair including a first metal conductor and a second metal conductor. Each bit line pair includes a reference bit line and a sense bit line. Each bit line pair may be configured such that the reference bit line and the sense bit line are longitudinally oriented with respect to each other. Alternatively, each bit line pair is configured such that the first metal conductor and the second metal conductor are symmetrically twisted about each other in at least one location. The lateral spacing between a cell plate and a transistor gate is minimized, resulting in reduced overall area.